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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,438	07/22/2004	Christopher Edward Gregory	033963-007	3681

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/502,438	GREGORY, CHRISTOPHER EDWARD	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the preliminary amendment filed 7/22/2004. Claims 6-13 are pending and are under examination.

Specification

1. The abstract of the disclosure is objected to because it includes "(Fig. 4)". It is suggested to delete it. Correction is required. See MPEP § 608.01(b).

Information Disclosure Statement

2. The information disclosure statement filed 11/23/2005 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (USP 6,452,433).

Figure 11 shows a latch circuit comprising a first latch portion including a first clock transistor (1114), a second latch portion including a second clock transistor (1112), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (A2) has a different property or characteristic to the second clock transistor (A1) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (A2 is multiple integers of A1) as called for in claims 6-9.

5. Claims 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Muller (USP 4,289,979).

Figure 1 shows a latch circuit comprising a first latch portion including a first clock transistor (T7), a second latch portion including a second clock transistor (T5), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (multiple emitters) has a different property or characteristic to the second clock transistor (single emitter) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (multiple emitter is multiple times bigger than a single emitter) as called for in claims 6-9.

6. Claims 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Denny (USP 4,922,127).

Figure 5 shows a latch circuit comprising a first latch portion including a first clock

transistor (T14), a second latch portion including a second clock transistor (T15), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (different size from T15) has a different property or characteristic to the second clock transistor (different size from T14r) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (size different in multiple integer n) as called for in claims 6-9.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (USP 6,452,433).

Figure 11 shows a latch circuit comprising a first latch portion including a first clock transistor (1114), a second latch portion including a second clock transistor (1112), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (A2) has a different property or characteristic to the second clock transistor (A1) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (A2 is multiple integers of A1).

Chang et al. does not disclose the latch circuit can be used in a prescaler circuit as called for in claims 10-13. However, it is notoriously well known in the art to implement a prescaler circuit with a master slave latch structure. Therefore, it would have been obvious to person

skilled in the art at the time the invention was made to include Chang et al.'s latch circuit in a prescaler circuit for the purpose of reducing operating power thus prolong a battery life.

9. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (USP 4,289,979).

Figure 1 shows a latch circuit comprising a first latch portion including a first clock transistor (T7), a second latch portion including a second clock transistor (T5), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (multiple emitters) has a different property or characteristic to the second clock transistor (single emitter) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (multiple emitter is multiple times bigger than a single emitter).

Muller does not disclose the latch circuit can be used in a prescaler circuit as called for in claims 10-13. However, it is notoriously well known in the art to implement a prescaler circuit with a master slave latch structure. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include Muller et al.'s latch circuit in a prescaler circuit for the purpose of minimizing untimely changes in states thus reducing erroneous operation.

10. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denny (USP 4,922,127).

Figure 5 shows a latch circuit comprising a first latch portion including a first clock transistor (T14), a second latch portion including a second clock transistor (T15), wherein the first and second clock transistors form a transistor clock pair and the first clock transistor (different size from T15) has a different property or characteristic to the second clock transistor

(different size from T14r) such that a ratio of a hold period to a follow period of the transistor clock pair is grater than 1 (size different in multiple integer n).

Danny does not disclose the latch circuit can be used in a prescaler circuit as called for in claims 10-13. However, it is notoriously well known in the art to implement a prescaler circuit with a master slave latch structure. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include Danny's latch circuit in a prescaler circuit for the purpose of minimizing untimely changes in states thus reducing erroneous operation.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art in the PTOL-1449 has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

1/7/2006